What is claimed is:

1. A system for controlling an international mobile telecommunications - 2000 (IMT-2000) base station, comprising:

a base transceiver station (BTS) for providing asynchronous transfer mode (ATM) cells;

an asynchronous transfer mode (ATM) switch for performing a switching of the ATM cells; and

a BTS interface subsystem (BIS) for interfacing the base transceiver station (BTS) with the asynchronous transfer mode (ATM) switch, wherein the BTS interface subsystem (BIS) includes a plurality of assembly symbol subsystems (ASSs) for receiving the ATM cells transmitted from the base transceiver station (BTS) and performing a type conversion of the ATM cells to output a type converted ATM cells to the asynchronous transfer mode (ATM) switch.

2. The system as recited in claim 1, wherein the ATM cells are transmitted from the base transceiver station (BTS) to the BTS interface subsystem (BIS) via E1 line.

3. The system as recited in claim 2, wherein each assembly symbol subsystem (ASS) includes:

a processor for controlling an operation of the assembly symbol subsystem (ASS);

a plurality of E1 interface units for restoring and encoding data transmitted via the E1 line to output E1 frame

data;

a plurality of ATM physical layer execution units for extracting ATM cells from the E1 frame data and performing an error correction operation to ATM cell header and a cell rate decoupling operation;

a reception (RX) multiplexer for classifying the ATM cells into first ATM cells corresponding to internal signals and second ATM cells corresponding to remaining ATM cells, wherein the first ATM cells are transmitted to the processor;

a reception (RX) type conversion unit for receiving the second ATM cells and classifying the second ATM cells into ATM adaptation layer 5 (AAL5) ATM cells and ATM adaptation layer 2 (AAL2) ATM cells, wherein the AAL5 ATM cells are bypassed to the reception (RX) multiplexer and the AAL2 ATM cells are converted into AAL2 prime ATM cells to transmit the AAL2 prime ATM cells to the reception (RX) type conversion unit;

a transmission (TX) multiplexer for outputting the first ATM cells and the second ATM cells, the first ATM cells being transmitted to the processor;

a transmission (TX) type conversion unit for classifying the second ATM cells transmitted from the transmission (TX) multiplexer into AAL5 ATM cells and AAL2 ATM cells, wherein the AAL5 ATM cells are bypassed to the transmission (TX) multiplexer, and the AAL2 ATM cells are converted into AAL2 prime ATM cells to transmit the AAL2 prime ATM cells to the transmission (TX) multiplexer;

a physical layer execution unit for performing a physical

layer function to the ATM cells at a predetermined speed, wherein the ATM cells are transmitted between the reception (RX) multiplexer and the optical transceiver; and

an optical transceiver for receiving data from the physical layer execution unit and transmitting the data to the ATM switch.

4. The system as recited in claim 3, wherein the ATM physical execution units transmit data to the BTS.

5. The system as recited in claim 4, wherein the optical transceiver receives data from the ATM switch and transmits the received data to the physical layer execution unit.

6. The system as recited in claim 5, wherein the number of the E1 interface units is determined by a total number of the E1 lines that is controlled by the ASS.

7. The system as recited in claim 6, wherein the E1 interface units include PM4313 chips, wherein the ATM physical layer execution units include PM7344 chips, and wherein the physical layer execution unit includes PM5346 chip, the PM4313 chip, the PM7344 chip and the PM5346 chip being provided by PMC-Sierra.

8. The system as recited in claim 7, wherein the predetermined speed is of 155 Mbps.